In re Patent Application of:
PEZZINI
Serial No. **10/634,150**
Filing Date: **AUGUST 4, 2003**
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In the Claims:

Claims 1-4 (Cancelled).

5. (Previously presented) A serial peripheral interface comprising:

a memory coupled to at least one data bus and an address bus, said memory for storing data from the at least one data bus associated with a plurality of peripheral devices based upon respective data addresses on the address bus, said memory having a respective transmit data section and a respective receive data section for each peripheral device and also having a configuration command section for storing configuration commands for use in communicating with each of the peripheral devices;

a data pointer for pointing to transmit and receive data section addresses;

a control register for controlling said data pointer based upon at least one configuration command associated with a selected peripheral device;

a data transfer circuit for serially transferring data between said memory and the selected peripheral device based upon the at least one configuration command; and

a configuration pointer for pointing to an address at which the at least one configuration command is stored in the configuration command section based upon a data address on the at least one data bus.

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6. (Previously presented) The serial peripheral interface of Claim 5 wherein said memory comprises a random access memory (RAM).

7. (Previously presented) The serial peripheral interface of Claim 5 wherein said configuration pointer comprises a random access memory (RAM).

8. (Previously presented) The serial peripheral interface of Claim 5 wherein the at least one data bus comprises a data reception bus for receiving data from the peripheral devices, and a data transmission bus for transferring data to the peripheral devices.

9. (Previously presented) A serial communication device comprising:

at least one data bus and an address bus;

a processor coupled to said at least one data bus and said address bus; and

a serial peripheral interface coupled to said processor and comprising

a memory coupled to said at least one data bus and said address bus, said memory for storing data from the at least one data bus associated with a plurality of peripheral devices based upon respective data addresses on the address bus, said memory having a respective transmit data section and a respective receive data

section for each peripheral device and also having a configuration command section for storing configuration commands for use in communicating with each of the peripheral devices,

a data pointer for pointing to transmit and receive data section addresses,

a control register for controlling said data pointer based upon at least one configuration command associated with a selected peripheral device,

a data transfer circuit for serially transferring data between said memory and the selected peripheral device based upon the at least one configuration command, and

a configuration pointer for pointing to an address at which the at least one configuration command is stored in the configuration command section based upon a data address on the at least one data bus.

10. (Previously presented) The serial communication device of Claim 9 wherein said memory comprises a random access memory (RAM).

11. (Previously presented) The serial communication device of Claim 9 wherein said configuration pointer comprises a random access memory (RAM).

12. (Previously presented) The serial communication

device of Claim 9 wherein the at least one data bus comprises a data reception bus for receiving data from the peripheral devices, and a data transmission bus for transferring data to the peripheral devices.

13. (Previously presented) A serial data transfer method comprising:

coupling a memory to at least one data bus and an address bus, the at least one data bus also being coupled to a plurality of peripheral devices, the memory having a respective transmit data section and a respective receive data section for each peripheral device and also having a configuration command section for storing configuration commands for use in communicating with each of the peripheral devices;

storing the configuration commands in the configuration command section;

determining an address at which at least one configuration command for a selected peripheral device is stored in the configuration command section based upon a data address on the at least one data bus; and

serially transferring data between the memory and the selected peripheral device based upon the at least one configuration command.

14. (Previously presented) The method of Claim 13 wherein the memory comprises a random access memory (RAM).

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15. (Previously presented) The method of Claim 13 wherein the at least one data bus comprises a data reception bus for receiving data from the peripheral devices, and a data transmission bus for transferring data to the peripheral devices.